TS128MQR72V5K

240PIN DDR2 533 Registered DIMM
1024MB With 128Mx4 CL4

Description

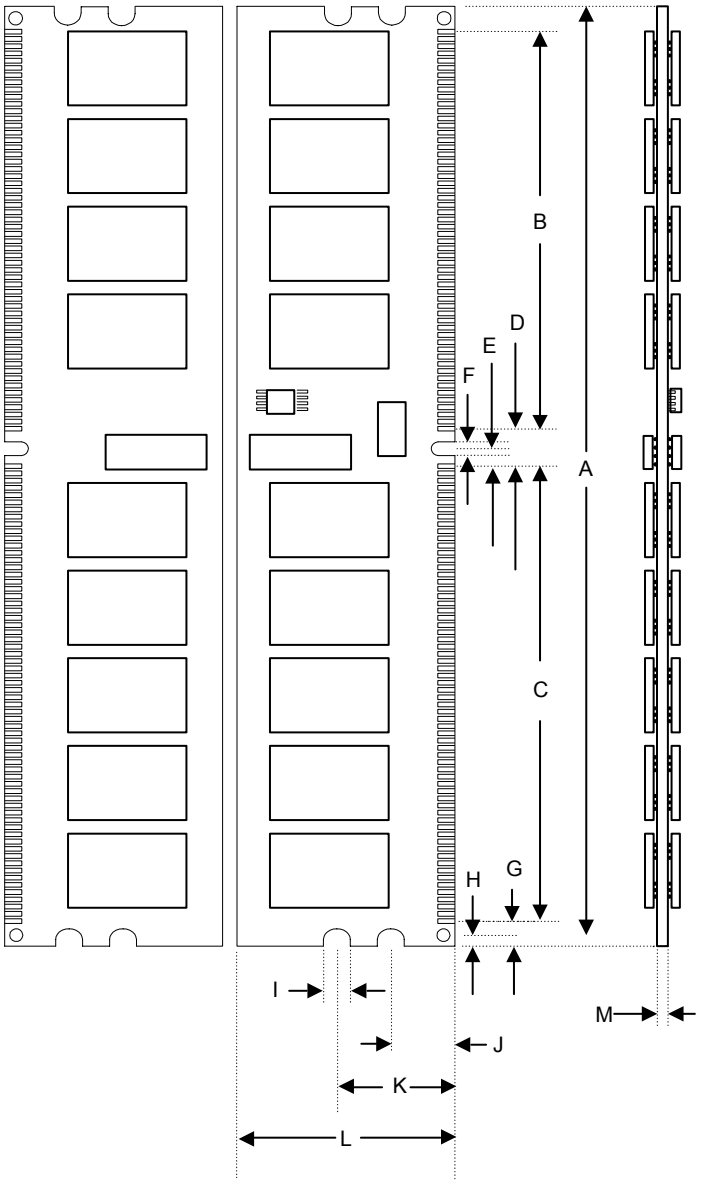
The TS128MQR72V5K is a 128M x 72bits DDR2-533 Registered DIMM. The TS128MQR72V5K consists of 18 pcs 128Mx4bits DDR2 SDRAMs in 60 ball FBGA package, 2 pcs register in 96 ball uBGA package, 1 pcs PLL driver IC and a 2048 bits serial EEPROM on a 240-pin printed circuit board. The TS128MQR72V5K is a Dual In-Line Memory Module and is intended for mounting into 240-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.8V ± 0.1V Power supply
- VDDQ=1.8V ± 0.1V
- Max clock Freq: 267MHZ; 533Mb/S/Pin.
- Posted CAS
- Programmable CAS Latency: 3,4,5
- Programmable Additive Latency :0, 1,2,3 and 4
- Write Latency (WL) = Read Latency (RL)-1
- Burst Length: 4,8(Interleave/nibble sequential)
- Programmable sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- MRS cycle with address key programs.
- On Die Termination
- Refresh and Self Refresh
  Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Serial presence detect with EEPROM

Placement



PCB: 09-2090

Dimensions

Side	Millimeters	Inches
A	133.35±0.15	5.250±0.006
B	55	2.165
C	63	2.480
D	5	0.197
E	2.5	0.098
F	1.5±0.10	0.059±0.039
G	5.175	0.204
H	2.2	0.867
I	4	0.157
J	10	0.394
K	17.8	0.701
L	30±0.15	1.181±0.006
M	1.27±0.10	0.050±0.004

(Refer Placement)

Pin Description

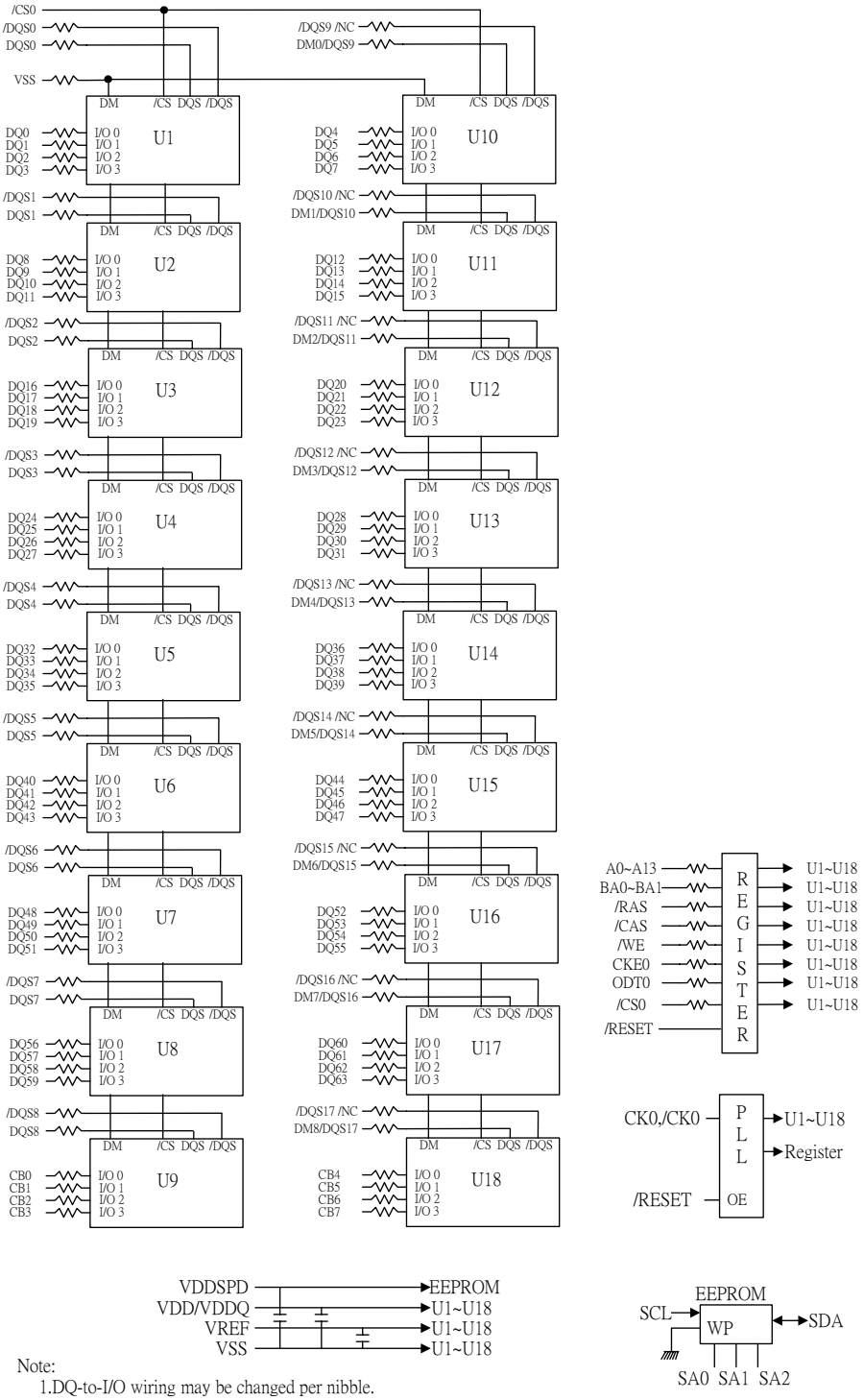
Symbol	Function
A0~A13, BA0, BA1	Address input, bank address
DQ0~DQ63	Data Input / Output.
CB0~CB7	Data Check Bits Input/Output
DQS0~DQS8	Data strobe
/DQS0~/DQS8	Data strobe , negative line
CK0, /CK0	Clock Input.
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM8	Data-in Mask
/DQS9~/DQS17	Data strobes(Read),negative line
VDD	+1.8 Voltage power supply
VDDQ	+1.8 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	Serial EEPROM Positive Power Supply
SA0~SA2	Address select for EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
/RESET	Register and PLL control pin
/Err_Out	Parity error found in the bus
Par_In	Parity bit for address and control bus
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	41	VSS	81	DQ33	121	VSS	161	*CB4	201	VSS
02	VSS	42	*CB0	82	VSS	122	DQ4	162	*CB5	202	*DM4,DQS13
03	DQ0	43	*CB1	83	/DQS4	123	DQ5	163	VSS	203	*NC,/DQS13
04	DQ1	44	VSS	84	DQS4	124	VSS	164	*DM8,DQS17	204	VSS
05	VSS	45	*/DQS8	85	VSS	125	*DM0,DQS9	165	*NC,/DQS17	205	DQ38
06	/DQS0	46	*DQS8	86	DQ34	126	*NC,/DQS9	166	VSS	206	DQ39
07	DQS0	47	VSS	87	DQ35	127	VSS	167	CB6	207	VSS
08	VSS	48	*CB2	88	VSS	128	DQ6	168	CB7	208	DQ44
09	DQ2	49	*CB3	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	CKE1	211	*DM5,DQS14
12	DQ8	52	CKE0	92	/DQS5	132	DQ13	172	VDD	212	*NC,/DQS14
13	DQ9	53	VDD	93	DQS5	133	VSS	173	NC	213	VSS
14	VSS	54	NC	94	VSS	134	*DM1,DQS10	174	NC	214	DQ46
15	/DQS1	55	*NC,Err_Out	95	DQ42	135	*NC,/DQS10	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	CK1	177	A9	217	DQ52
18	NC	58	A7	98	DQ48	138	/CK1	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	VSS	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	CK2
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ	221	/CK2
22	DQ11	62	VDDQ	102	NC	142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	*DM6,DQS15
24	DQ16	64	VDD	104	/DQS6	144	DQ21	184	VDD	224	*NC,/DQS15
25	DQ17	65	VSS	105	DQS6	145	VSS	185	CK0	225	VSS
26	VSS	66	VSS	106	VSS	146	*DM2,DQS11	186	/CK0	226	DQ54
27	/DQS2	67	VDD	107	DQ50	147	*NC,/DQS11	187	VDD	227	DQ55
28	DQS2	68	NC	108	DQ51	148	VSS	188	A0	228	VSS
29	VSS	69	VDD	109	VSS	149	DQ22	189	VDD	229	DQ60
30	DQ18	70	A10/AP	110	DQ56	150	DQ23	190	BA1	230	DQ61
31	DQ19	71	BA0	111	DQ57	151	VSS	191	VDDQ	231	VSS
32	VSS	72	VDDQ	112	VSS	152	DQ28	192	/RAS	232	*DM7,DQS16
33	DQ24	73	/WE	113	/DQS7	153	DQ29	193	/CS0	233	*NC,/DQS16
34	DQ25	74	/CAS	114	DQS7	154	VSS	194	VDDQ	234	VSS
35	VSS	75	VDDQ	115	VSS	155	*DM3,DQS12	195	ODT0	235	DQ62
36	/DQS3	76	/CS1	116	DQ58	156	*NC,/DQS12	196	A13	236	DQ63
37	DQS3	77	ODT1	117	DQ59	157	VSS	197	VDD	237	VSS
38	VSS	78	VDDQ	118	VSS	158	DQ30	198	VSS	238	VDDSPD
39	DQ26	79	VSS	119	SDA	159	DQ31	199	DQ36	239	SA0
40	DQ27	80	DQ32	120	SCL	160	VSS	200	DQ37	240	SA1

*Please refer Block Diagram

Block Diagram



Note:
1.DQ-to-I/O wiring may be changed per nibble.
2.Unless otherwise noted , resister values are 22 Ohms±5%

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on V_{DD} relative to Vss	VDD	-1.0 ~ 2.3	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.5 ~ 2.3	V	1
Voltage on V_{DDL} pin relative to Vss	VDDL	-0.5 ~ 2.3	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 2.3	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2
Mean time between failure	MTBF	Reserved	year	
Temperature Humidity Burning	THB	Reserved	°C-%	
Temperature Cycling Test	TC	Reserved	°C	

Note:
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.8)

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.7	1.8	1.9	V	
Supply voltage for DLL	VDDL	1.7	1.8	1.9	V	4
Supply voltage for Output	VDDQ	1.7	1.8	1.9	V	4
I/O Reference voltage	VREF	0.49*V_{DDQ}	0.50*VDDQ	0.51*V_{DDQ}	V	1,2
I/O Termination voltage	VTT	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
DC Input logic high	$V_{IH(DC)}$	V_{REF}+0.125	-	V_{DDQ}+0.3	V	
DC Input logic low	$V_{IL(DC)}$	-0.3	-	V_{REF}-0.125	V	

Note:
There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed +/-2% VREF (DC).
3. VTT of transmitting device must track VREF of receiving device.
4. AC parameters are measured with VDD, VDDQ and VDDDL tied together.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 95	°C	1,2,3

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

IDD Specification parameters Definition

(IDD values are for full operating range of voltage and Temperature)

Parameter		Symbol	Max.	Unit	Note
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD0	1,350	mA	
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		IDD1	1,530	mA	
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P	90	mA	
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2Q	450	mA	
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD2N	540	mA	
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	IDD3P-F	360	mA	
	Slow PDN Exit MRS(12) = 1mA	IDD3P-S	108		
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD3N	540	mA	
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		IDD4R	2070	mA	
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R		IDD4W	2,250	mA	
Burst Auto refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD5B	2,970	mA	
Self refresh current; CK and CK\ at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		IDD6	90	mA	
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK =tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		IDD7	4,140	mA	

Note: 1. Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading capacitor.

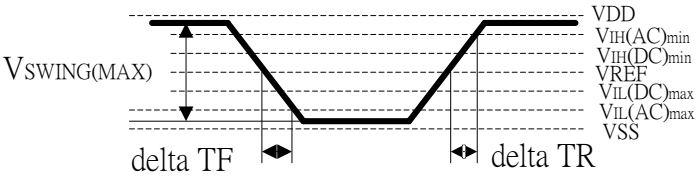
Input AC Logic Level

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.250		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.250	V	

AC Input Test Condition

Condition	Symbol	Value	Unit	Note
Input reference voltage	VREF	0.5*VDDQ	V	1
Input signal maximum peak to peak swing	VSWING(MAX)	1.0	V	1
Input signal minimum slew rate	SLEW	1.0	V/ns	2,3

Note: 1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) min for rising edges and the range from VREF to VIL(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.



$$\text{Falling Slew} = \frac{V_{REF} - V_{IL}(AC)_{max}}{\text{delta TF}} \qquad \text{Rising Slew} = \frac{V_{IH}(AC)_{min} - V_{REF}}{\text{delta TR}}$$

AC Input Test Signal Waveform

Input/Output Capacitance (V_{DD} = 1.8V, V_{DDQ} = 1.8V, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input capacitance (CK and /CK)	CCK	-	11	pF
Input capacitance (CKE0 and /CS)	CI_1	-	12	pF
Input capacitance (A0~A12, BA0~BA1, /RAS, /CAS, /WE)	CI_2	-	12	pF
Input capacitance (DQ, DM, DQS, /DQS)	CIO	-	10	pF

Note: DM is internally loaded to match DQ and DQS identically.

Timing Parameters & Specifications

(These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Unit	Note
DQ output access time from CK & /CK	tAC	-500	+500	ps	
DQS output access time from CK & /CK	tDQSCK	-450	+450	ps	
CK high-level width	tCH	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	X	ps	
Clock cycle time, CL=x	tCK	3750	8000	ps	
DQ and DM input hold time	tDH	225	x	ps	
DQ and DM input setup time	tDS	100	X	ps	
Control & Address input pulse width for each input	tIPW	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	X	tCK	
Data-out high-impedance time from CK/CK	tHZ	X	tAC max	ps	
DQS low-impedance time from CK/CK	tLZ(DQS)	tAC min	tAC max	ps	
DQ low-impedance time from CK/CK	tLZ(DQ)	2*tAC min	TACmax	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	X	300	ps	
DQ hold skew factor	tQHS	X	400	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	X	ps	
Write command to first DQS latching transition	tDQSS	WL-0.25	WL+0.25	tCK	
DQS input high pulse width	tDQSH	0.35	X	tCK	
DQS input low pulse width	tDQSL	0.35	X	tCK	
DQS falling edge to CK setup time	tDSS	0.2	X	tCK	
DQS falling edge hold time from CK	tDSH	0.2	X	tCK	
Mode register set command cycle time	tMRD	2	X	tCK	
Write postamble	tWPST	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	X	tCK	
Address and control input hold time	475	375	X	ps	
Address and control input setup time	tIS	250	X	ps	
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
Active to active command period for 1KB page size products	tRRD	7.5	X	ns	
Active to active command period for 2KB page size products	tRRD	10	X	ns	
Four Activate Window for 1KB page size products	tFAW	37.5		ns	

Four Activate Window for 2KB page size products	tFAW	50		ns	
/CAS to /CAS command delay	tCCD	2		tCK	
Write recovery time	tWR	15	X	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP	X	tCK	
Internal write to read command delay	tWTR	7.5	X	ns	
Internal read to precharge command delay	tRTP	7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200		tCK	
Exit precharge power down to any non-read command	tXP	2	X	tCK	
Exit active power down to read command	tXARD	2	X	tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		tCK	
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max)+1	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		tCK	
ODT power down exit latency	tAXPD	8		tCK	
OCD drive mode output delay	tOIT	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		ns	

SERIAL PRESENCE DETECT SPECIFICATION

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Serial PD Bytes written during module production	128bytes	80
1	Total # of Bytes of S.P.D Memory Device	256bytes	08
2	Fundamental Memory Type	DDR2 SDRAM	08
3	# of Row Addresses on this Assembly	14	0E
4	# of Column Addresses on this Assembly	11	0B
5	# of Module Rows on this Assembly	1 ROW, Planar, 30.0mm	60
6	Data Width of this Assembly	72bits	48
7	Reserved	-	00
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V	05
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	3.75ns	3D
10	DDR2 SDRAM Access time from clock at CL=X	±0.5ns	50
11	DIMM configuration type (non-parity, Parity, ECC)	ECC	02
12	Refresh Rate	7.8us	02
13	Primary DDR2 SDRAM Width	X4	04
14	Error Checking DDR2 SDRAM Width	X4	04
15	Reserved	-	00
16	DDR2 SDRAM device attributes: Burst lengths supported	4,8	0C
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	4 banks	04
18	DDR2 SDRAM device attributes:CAS Latency supported	5,4,3	38
19	Reserved	-	00
20	DIMM type information	Regular RDIMM	01
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable	00
22	DDR2 SDRAM Device Attributes: General	Supports weak driver	01
23	DDR2 SDRAM Cycle Time CL=X-1	3.75ns	3D
24	DDR SDRAM Access from Clock CL=X-1	±0.5ns	50
25	DDR SDRAM Cycle Time CL=X-2	5.0ns	50
26	DDR SDRAM Access from Clock CL=X-2	±0.6ns	60
27	Minimum Row Precharge Time (tRP)	15ns	3C
28	Minimum Row Active to Row Activate delay (tRRD)	7.5ns	1E
29	Minimum RAS to CAS Delay (tRCD)	15ns	3C
30	Minimum active to Precharge time (tRAS)	40ns	28
31	Module ROW density	1GB	01
32	Command and address setup time before clock(=tIS)	0.25ns	25
33	Command and address hold time after clock(=tIH)	0.37ns	37
34	Data input setup time before strobe(=tDS)	0.10ns	10
35	Data input hold time after strobe(=tDH)	0.22ns	22
36	Write recovery time(=tWR)	15ns	3C

37	Internal write to read command delay(=tWTR)	7.5ns	1E					
38	Internal read to precharge command delay(=tRTP)	7.5ns	1E					
39	Memory analysis probe characteristics	-	00					
40	Reserved	-	00					
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	55ns	37					
42	DDR SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	105ns	69					
43	DDR SDRAM Maximum Device Cycle Time (tCK max)	8ns	80					
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.3ns	1E					
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	0.4ns	28					
46	PLL Relock Time	15us	0F					
47~61	Superset Information	-	00					
62	SPD Data Revision Code	REV 1.0	10					
63	Checksum for Bytes 0-62	-	C0					
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS128MQR72V5K	54	53	31	32	38	4D
			51	52	37	32	56	35
			4B	20	20	20	20	20
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Open for customer use	Undefined	-					